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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,765	08/28/2003	Teruhisa Obara	OKI 368	5864

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RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER
SIDDIQUI, SAQIB JAVAID

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,765	OBARA, TERUHISA	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered June 12, 2006.

- Claims 1-12 are pending. Claims 1-3 & 7-12 are amended.
- Claims 13-14 are canceled.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to amended claims 1-3, 7-12 and previously presented claims 2-6 filed June 12, 2006 have been considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends that Whetsel's scan path does not teach a first logic circuit having a data input terminal, a first scan register connected to the first logic circuit, the first scan register having a test input register and a last scan register having an output terminal. In addition applicant contends that Whetsel's scan path does not say that it includes logic circuit alternating with san registers. The examiner respectfully disagrees.

Te definition of scan path as found in the computing dictionary: *"A technique used to increase the controllability and observability of a logic circuit by incorporating scan registers into the circuit. Normally these act like flip-flops but they can be switched into a "test" mode where they all become one long shift register. This allows data to be clocked serially through all the scan registers and out of an output pin at the same time as new data is clocked in from an input pin."* As evident by the definition one can clearly

see that a scan path includes both logic circuits and scan registers that are connected in series as data is being serially shifted through them. In addition, the first register and last registers in the scan path will serve as the first and last registers in the scan path.

Secondly, applicant contends that it would not be useful to one of ordinary skill in the art at the time the invention was made to use a multiplied clock signal in Whetsel's invention. The examiner respectfully disagrees.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Whetsel's invention partitions the functional circuitry into many shorter scan path in order to reduce the test time of the integrated circuit (column 2, lines 2-65). In addition, "the number of available bond pad pairs will limit the number of scan paths that can be accessed in parallel" (column 3, lines 1-15). By combining the two inventions, and enabling Whetsel's invention to use a multiplied clock signal, clock signals of different frequencies could be sent through scan paths of different lengths, without increasing the testing time. Hence, Whetsel's invention will not be limited to testing short scan paths, or by the number of available bond pairs.

As per the rejections under Kobayashi, the applicant contends that Kobayashi does not represent a plurality of logic circuits and a plurality of scan registers connected alternately in series, and Kobayashi's serial/parallel and parallel/serial conversion circuits are located opposite to what is recited in the claims. Given the broadest possible interpretation of the term "logic circuits", register number 121 can be interpreted as a logic circuit, and hence the path from 120-123 overcomes the limitation a plurality of logic circuits and a plurality of scan registers connected alternately in series. As per the opposite location of the converters it has been held that that a mere reversal of the essential working parts of a device involves only routine skill in the art. *In re Einstein*, 8 USPQ 167.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel US Pat no. 6,242,269 B1, and further in view of Eriksson et al. US Patent no. 6,169,500 B1

As per claim 1:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising: m scan chains (wherein m is an integer greater than 1) each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal and the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal.

However, Eriksson et al. in an analogous art; teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal

(Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 2:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising: m scan chains (wherein m is an integer greater than 1) each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a

serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67), further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 2, lines 3-13).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal, the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal, and the multiplication circuit generating the multiplied clock signal based on the clock signal received thereto.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"), and further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 1, lines 31-33), the multiplication circuit generating the multiplied clock signal based on the clock signal received thereto (column 2 lines 54-60). Therefore it would have been

obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claims 3-5:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising: m scan chains (wherein m is an integer greater than 1) each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67), further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 2, lines 3-13), wherein the serial/parallel conversion circuit including a plurality of flip-flops

connected in series (column 4, lines 54-61), and a plurality of selectors (Figure 8 # 876, column 7, lines 64-67), wherein each of the serial registers includes a selector and a flip-flop.

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal, the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal, and wherein each of the serial registers includes a selector and a flip-flop being operated in response to the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"), and wherein each of the serial registers includes a selector and a flip-flop being operated in response to the clock signal (Figure 6 #71 a-f, "CLK184a-d") .

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan

chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 6:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising: m scan chains (wherein m is an integer greater than 1) each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series (Figure 8 # 924), each of the scan chains including a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67), wherein the output terminal of the last scan register of one of the scan chains (Figure 8 # 946) is connected to the data input terminal of the first logic circuit of another one of the scan chains (Figure 8, # 964 and "PSC").

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal and the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 7:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising a plurality of scan chains each of which includes a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a

serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal and the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in

relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 8:

Whetsel teaches a semiconductor integrated circuit (Figure 8 # 700) comprising a plurality of scan chains each of which includes a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67), further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 2, lines 3-13).

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal, the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal, and the multiplication circuit generating the multiplied clock signal based on the clock signal received thereto.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 “CLK”, column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50

a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"), and further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 1, lines 31-33), the multiplication circuit generating the multiplied clock signal based on the clock signal received thereto (column 2 lines 54-60). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claims 9-11:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising a plurality of scan chains each of which includes a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a

serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67), further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit (column 2, lines 3-13), wherein the serial/parallel conversion circuit including a plurality of flip-flops connected in series (column 4, lines 54-61), and a plurality of selectors (Figure 8 # 876, column 7, lines 64-67), wherein each of the serial registers includes a selector and a flip-flop.

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal, the conversion circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal, and wherein each of the serial registers includes a selector and a flip-flop being operated in response to the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 “CLK”, column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, “CLK184a-c”); the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, “CLK184d”), and wherein each of the serial registers includes a selector and a flip-flop

being operated in response to the clock signal (Figure 6 #71 a-f, "CLK184a-d") .

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

As per claim 12:

Whetsel substantially teaches a semiconductor integrated circuit (Figure 8 # 700) comprising a plurality of scan chains each of which includes a first logic circuit having a data input terminal (Figure 8 # 800, column 7, lines 53-56), a first scan register connected to the first logic circuit (Figure 8 # 800, column 7, lines 53-56), the first scan register having a test input terminal (Figure 8 # 900, column 8, lines 6-8), and a last scan register having an output terminal (Figure 8 # 844, column 7, lines 58-61); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (column 1, lines 65-66), and a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains (column 1, lines 66-67), wherein the selectors of the serial registers are operated in response to a mode signal (Figure 10 "MUX").

Whetsel does not explicitly teach a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal and the conversion

circuits converting data in response to a multiplied clock signal having a frequency being m times of that of the clock signal.

However, Eriksson et al. in an analogous art, teaches a semiconductor integrated circuit wherein; the scan registers are being operated in response to a clock signal (Figure 2 "CLK", column 2, lines 54-56), the serial/parallel conversion circuit (Fig 6 # 50 a-c) converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 6, "CLK184a-c"); and the parallel/serial conversion circuit (Fig 6 # 60) converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Fig 6, "CLK184d"). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use clock signal within to control the operations of the scan chains and conversion circuits in the teaching of Whetsel. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that using a clock signal to control the operation of a scan chain is a commonplace practice in the art and delaying the incoming signals in relation to the clock signals will reduce the risk of errors (Eriksson et al., column 1, lines 53-56).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 & 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi US PG-Pub no. 2003/0056183 A1.

As per claim 1:

Kobayashi substantially teaches a semiconductor integrated circuit (Figure 1) comprising: m scan chains (wherein m is an integer greater than 1) each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series (Figure 1(a) # 120-123), the scan registers being operated in response to a clock signal (Figure 1(b) "SC_CLOCK", paragraph [0037]), each of the scan chains including a first logic circuit having a data input terminal (Figure 1(a) #10), a first scan register connected to the first logic circuit (Figure 1(a) "SIN0"), the first scan register having a test input terminal (Figure 1(b) "SCAN IN"), and a last scan register having an output terminal (Figure 1(a) "SOUT0"); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (Figure 1(a) # 11, paragraph [0035], lines 8-12), the serial/parallel conversion circuit converting serial data into parallel data in response to a multiplied clock signal having a

frequency being m times of that of the clock signal (Figure 4 "SC_CLOCK", paragraph [0043], lines 5-12); and a parallel/serial conversion circuit (Figure 1(a) # 10, paragraph [0035], lines 4-8), the parallel/serial conversion circuit converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Figure 3 "SC_CLOCK", paragraph [0040], lines 1-10).

Kobayashi does not teach the exact location of the parallel/serial converter, as disclosed in the specification. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to place the parallel/serial converter at the output terminal of the invention, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse, 86 USPQ 70.*

As per claim 7:

Kobayashi substantially teaches a semiconductor integrated circuit (Figure 1) comprising: a plurality of scan chains (Figure 1(a) "SIN0-3") each of which includes a first logic circuit having a data input terminal (Figure 1(b) "SCAN IN"), a first scan register connected to the first logic circuit (Figure 1(a) "SIN0"), the first scan register having a test input terminal (Figure 1(b) "SCAN IN"), and a last scan register having an output terminal (Figure 1(a) "SOUT0"); a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains (Figure 1(a) # 11, paragraph [0035], lines 8-12), the serial/parallel conversion circuit converting serial data into parallel data in response to a multiplied clock signal having a frequency being m times of that of the clock signal (Figure 4 "SC_CLOCK", paragraph [0043], lines 5-12); and a parallel/serial conversion circuit (Figure 1(a) # 10, paragraph [0035], lines 4-

8), the parallel/serial conversion circuit converting parallel data received from the scan chains into serial data in response to the multiplied clock signal (Figure 3 "SC_CLOCK", paragraph [0040], lines 1-10).

Kobayashi does not teach the exact location of the parallel/serial converter, as disclosed in the specification. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to place the parallel/serial converter at the output terminal of the invention, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse, 86 USPQ 70.*

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 6,466,247 B1 US Pat no. 6,014,763 and US Pat no. 5,978,870 mention the same test method using serial and parallel converters and having a clock means are included herein for Applicant's review.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to the final action is set to expire in THREE MONTH from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory

action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
08/13/06

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100